Having thus described the preferred embodiment, the invention is now claimed to be:

1. A method of forming a MOS transistor comprising the steps of:

a) forming a gate structure on a substrate with an upper layer of a hard mask material;

b) etching the hard mask material to remove a portion of the hard mask material and form a contoured mask on the gate structure, the contoured mask varying in thickness across the gate structure; and

c) implanting a halo dopant through the contoured mask into the substrate to form a halo implant.

2. The method of claim 1, further including prior to step b):

patterning the layer of hard mask material with a layer of photoresist material and removing an unpatterned portion of the hard mask material and gate layers to define the gate.

3. The method of claim 1, further including:

implanting a source/drain dopant into the substrate to form a source region and a drain region adjacent the gate.

4. The method of claim 3, wherein the step of forming the halo implant is carried out prior to the step of implanting the source/drain dopant.

5. The method of claim 1, wherein the step of forming the halo implant includes implanting the halo dopant at an implant angle of less than 30 degrees from an axis which is perpendicular to the surface of the substrate.

6. The method of claim 5, wherein the implant angle is up to about seven degrees from the perpendicular axis.

7. The method of claim 6, wherein the implant angle is generally perpendicular to the surface of the substrate.

8. The method of claim 1, wherein the step of etching the hard mask material includes anisotropically etching the hard mask material.

9. The method of claim 1, wherein the mask, after etching, has a contour which is thinner adjacent a peripheral edge of the gate and increases in thickness away from the peripheral edge.

10. The method of claim 9, wherein the step of implanting a halo dopant includes selecting the energy of the dopant such that the dopant penetrates the gate into the substrate at ends of a channel region defined under the gate, without penetrating the gate in a central portion of the channel.

11. The method of claim 1, wherein the hard mask material is silicon dioxide.

12. A method of forming a MOS device, the method comprising:

a) growing a gate oxide layer on a surface of a silicon substrate;

b) depositing a layer of polysilicon on the gate oxide layer;

c) forming a layer of a hard mask material on an upper surface of the polysilicon;

d) anisotropically etching the hard mask material to contour the hard mask material; and

e) implanting a halo dopant into the substrate through the contoured hard mask material at an implant angle which is less than about seven degrees from normal to the surface of the substrate to form a halo implant.

13. The method of claim 12, wherein halo dopant has an energy which is sufficient to penetrate the polysilicon gate structure only in regions adjacent a periphery of the gate structure.

14. The method of claim 13, further including:

implanting a source/drain dopant into the substrate of a conductivity type opposite to a conductivity type of the halo dopant to define source and drain regions adjacent opposite sides of the gate structure.

15. A MOS device comprising:

a gate structure on a semiconductor substrate, the gate structure having an upper layer of a hard mask material, the hard mask material being contoured such that it varies in thickness across the gate structure; and

a halo implant in the semiconductor substrate, the halo implant having a depth profile under the gate structure which follows the contour of the hard mask layer.

16. The device of claim 15, wherein the hard mask layer is a layer of silicon oxide.

17. The device of claim 15, wherein the hard mask layer has a convex upper surface.

18. The device of claim 15, wherein the halo implant is formed by a process which includes implanting a halo dopant into the substrate through the hard mask material at an implant angle which is generally perpendicular to the surface of the substrate.

19. The device of claim 15, wherein the gate structure includes a layer of polysilicon.

20. A MOS device formed by the process of either one of **claims 1 and 12.**